# **Freescale Semiconductor**

MPX2053 Rev 7, 10/2008

# 50 kPa On-Chip Temperature Compensated and Calibrated Silicon Pressure Sensors

The MPX2053 series devices are silicon piezoresistive pressure sensors that provide a highly accurate and linear voltage output directly proportional to the applied pressure. A single, monolithic silicon diaphragm with the strain gauge and an integrated thin-film resistor network. Precise span and offset calibration with temperature compensation are achieved by laser trimming.

#### **Features**

- Temperature Compensated Over 0°C to +85°C
- Easy-to-Use Chip Carrier Package Options
- · Ratiometric to Supply Voltage
- · Gauge Ported and Non Ported Options
- Available in Easy-to-Use Tape & Reel
- Differential and Gauge Pressure Options

# MPX2053 Series

0 to 50 kPa (0 to 7.25 psi) 40 mV Full Scale (Typical)

# **Application Examples**

- Pump/Motor Control
- Robotics
- Level Detectors
- Medical Diagnostics
- · Pressure Switching
- · Blood Pressure Measurement

			ORDE	RING INFO	RMATION				
Device Name	Case No.		# of Ports			Pressure Type		Device Marking	
Device Name	Case No.	None	Single	Dual	Gauge	Differential	Absolute	Device Marking	
Small Outline Pac	Small Outline Package (MPXV2053G Series)								
MPXV2053GP	1369		•		•			MPXV2053GP	
MPXV2053DP	1351			•		•		MPXV2053DP	
MPXV2053GVP	1368		•		•			MPXV2053GV	
Unibody Package	(MPX2053 S	eries)						•	
MPX2053D	344	•				•		MPX2053D	
MPX2053DP	344C			•		•		MPX2053DP	
MPX2053GP	344B		•		•			MPX2053GP	
MPAK Package (M	IPXM2053 Se	eries)							
MPXM2053D	1320	•				•		MPXM2053D	
MPXM2053DT1	1320	•				•		MPXM2053D	
MPXM2053GS	1320A		•		•			MPXM2053GS	
MPXM2053GST1	1320A		•		•			MPXM2053GS	



## **UNIBODY PACKAGES**



MPX2053D CASE 344-15



MPX2053GP CASE 344B-01



MPX2053DP CASE 344C-01

## **SMALL OUTLINE PACKAGES**



MPXV2053GP CASE 1368-01



MPXV2053GP CASE 1369-01



MPXV2053DP CASE 1351-01

# **MPAK PACKAGES**



MPXM2053D/DT1 CASE 1320-02



MPXM2053GS/GST1 CASE 1320A-02

# **Operating Characteristics**

Table 1. Operating Characteristics ( $V_S = 10 V_{DC}$ ,  $T_A = 25$ °C unless otherwise noted, P1 > P2)

Characteristic	Symbol	Min	Тур	Max	Units
Pressure Range <sup>(1)</sup>	P <sub>OP</sub>	0	_	50	kPa
Supply Voltage <sup>(2)</sup>	Vs	_	10	16	$V_{DC}$
Supply Current	Io	_	6.0	_	mAdc
Full Scale Span <sup>(3)</sup>	V <sub>FS</sub>	38.5	40	41.5	mV
Offset <sup>(4)</sup>	_	-1.0	_	1.0	mV
Sensitivity	_	ΔV/ΔΡ	_	0.8	_
Non-Linearity	_	-0.6	_	0.4	%V <sub>FS</sub>
Pressure Hysteresis (0 to 50 kPa)	_	_	±0.1	_	%V <sub>FS</sub>
Temperature Hysteresis (-40° to 125°C)	_	_	±0.5	_	%V <sub>FS</sub>
Temperature Coefficient of Full Scale	TCV <sub>FS</sub>	-2.0	_	2.0	%V <sub>FS</sub>
Temperature Coefficient of Offset	TCV <sub>OFF</sub>	-1.0	_	1.0	mV
Input Impedance	Z <sub>IN</sub>	1000	_	2500	Ω
Output Impedance	Z <sub>OUT</sub>	1400	_	3000	Ω
Response Time <sup>(5)</sup> (10% to 90%)	t <sub>R</sub>	_	1.0	_	ms
Warm-Up Time	_	_	20	_	ms
Offset Stability <sup>(6)</sup>	_	_	±0.5	_	%V <sub>FS</sub>

<sup>1. 1.0</sup> kPa (kiloPascal) equals 0.145 psi.

- 2. Device is ratiometric within this specified excitation range. Operating the device above the specified excitation range may induce additional error due to device self-heating.
- 3. Full Scale Span (V<sub>FSS</sub>) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.
- 4. Offset ( $V_{\rm off}$ ) is defined as the output voltage at the minimum rated pressure.
- 5. Response Time is defined as the time for the incremental change in the output to go from 10% to 90% of its final value when subjected to a specified step change in pressure.
- 6. Offset stability is the product's output deviation when subjected to 1000 hours of Pulsed Pressure, Temperature Cycling with Bias Test.

# **Maximum Ratings**

Table 2. Maximum Ratings<sup>(1)</sup>

Rating	Max Value	Unit
Supply Voltage	16	V
Pressure (P1 > P2)	200	kPa
Storage Temperature	-40 to +125	°C
Operating Temperature Range	-40 to +125	°C

1. Exposure beyond the specified limits may cause permanent damage or degradation to the device.

Figure 1 shows a block diagram of the internal circuitry integrated on a pressure sensor chip.

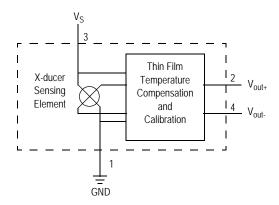


Figure 1. Temperature Compensated Pressure Sensor Schematic

# **Voltage Output versus Applied Differential Pressure**

The differential voltage output of the sensor is directly proportional to the differential pressure applied.

The output voltage of the differential or gauge sensor increases with increasing pressure applied to the pressure

side relative to the vacuum side. Similarly, output voltage increases as increasing vacuum is applied to the vacuum side relative to the pressure side.

# **On-Chip Temperature Compensation and Calibration**

Figure 2 shows the minimum, maximum and typical output characteristics of the MPX2053 series at 25°C. The output is directly proportional to the differential pressure and is essentially a straight line.

A silicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm.

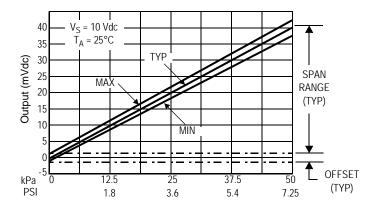


Figure 2. Output vs. Pressure Differential

#### **LINEARITY**

Linearity refers to how well a transducer's output follows the equation:  $V_{out} = V_{off} + \text{sensitivity x P}$  over the operating pressure range. There are two basic methods for calculating nonlinearity: (1) end point straight line fit (see Figure 3) or (2) a least squares best line fit. While a least squares fit gives the "best case" linearity error (lower numerical value), the calculations required are burdensome.

Conversely, an end point fit will give the "worst case" error (often more desirable in error budget calculations) and the calculations are more straightforward for the user. The specified pressure sensor linearities are based on the end point straight line method measured at the midrange pressure.

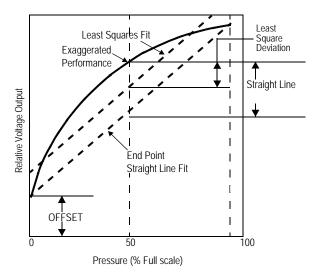


Figure 3. Linearity Specification Comparison

Figure 4 illustrates the differential or gauge configuration in the basic chip carrier (Case 344). A silicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm.

The MPX2053 series pressure sensor operating characteristics and internal reliability and qualification tests

are based on use of dry air as the pressure media. Media other than dry air may have adverse effects on sensor performance and long term reliability. Contact the factory for information regarding media compatibility in your application. Refer to application note AN3728, for more information regarding media compatibility.

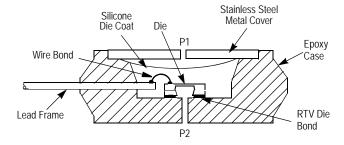
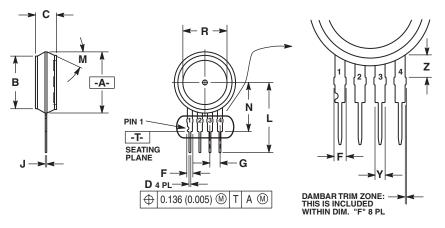


Figure 4. Unibody Package — Cross-Sectional Diagram (Not to Scale)



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION -A- IS INCLUSIVE OF THE MOLD STOP RING, MOLD STOP RING NOT TO EXCEED. 16.00 (0.630).

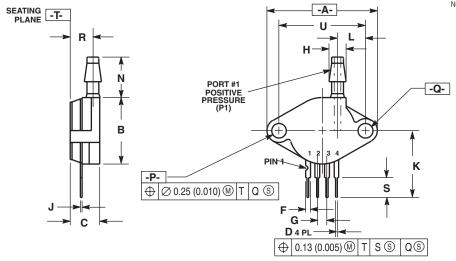
	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.595	0.630	15.11	16.00	
В	0.514	0.534	13.06	13.56	
С	0.200	0.220	5.08	5.59	
D	0.016	0.020	0.41	0.51	
F	0.048	0.064	1.22	1.63	
G	0.100	BSC	2.54 BSC		
J	0.014	0.016	0.36	0.40	
L	0.695	0.725	17.65	18.42	
M	30°	NOM	1 °08	MOV	
N	0.475	0.495	12.07	12.57	
R	0.430	0.450	10.92	11.43	
Υ	0.048	0.052	1.22	1.32	
Z	0.106	0.118	2.68	3.00	

STYLE 1:
PIN 1. GROUND
2. + OUTPUT
3. + SUPPLY
4. - OUTPUT

STYLE 2: PIN 1. Vcc 2. - SUPPLY 3. + SUPPLY 4. GROUND

STYLE 3: PIN 1. GND 2. -VOUT 3. VS 4. +VOUT

#### **CASE 344-15 ISSUE AA UNIBODY PACKAGE**



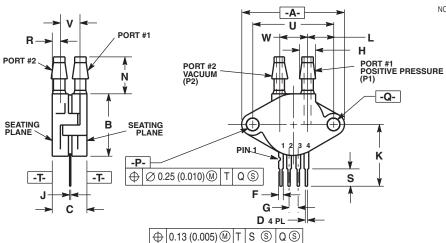
# NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: INCH.

	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	1.145	1.175	29.08	29.85
В	0.685	0.715	17.40	18.16
C	0.305	0.325	7.75	8.26
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100	BSC	2.54 BSC	
Н	0.182	0.194	4.62	4.93
J	0.014	0.016	0.36	0.41
K	0.695	0.725	17.65	18.42
L	0.290	0.300	7.37	7.62
N	0.420	0.440	10.67	11.18
Р	0.153	0.159	3.89	4.04
Ø	0.153	0.159	3.89	4.04
R	0.230	0.250	5.84	6.35
S	0.220	0.240	5.59	6.10
U	0.910	BSC	23.11	BSC

STYLE 1: PIN 1. GROUND 2. + OUTPUT 3. + SUPPLY 4. - OUTPUT

**CASE 344B-01 ISSUE B UNIBODY PACKAGE** 



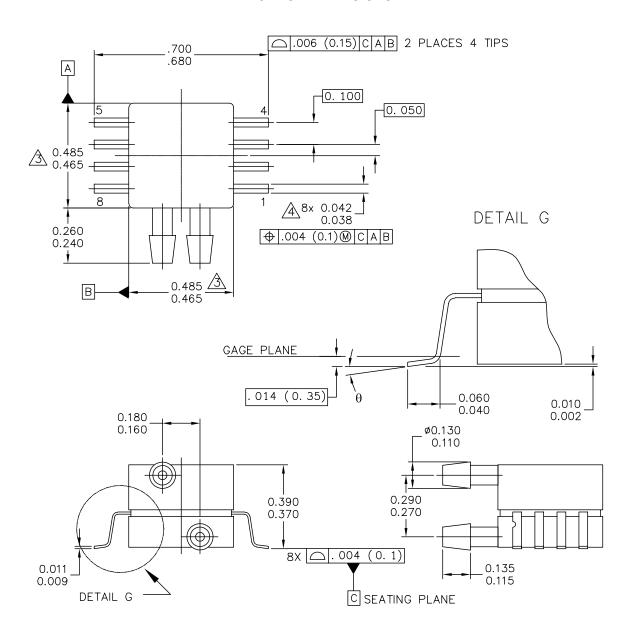
- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

	INC	HFS	MILLIN	IETERS
ым	MIN	MAX	MIN	MAX
Α	1.145	1.175	29.08	29.85
В	0.685	0.715	17.40	18.16
С	0.405	0.435	10.29	11.05
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
Н	0.182	0.194	4.62	4.93
J	0.014	0.016	0.36	0.41
K	0.695	0.725	17.65	18.42
L	0.290	0.300	7.37	7.62
N	0.420	0.440	10.67	11.18
Р	0.153	0.159	3.89	4.04
Q	0.153	0.159	3.89	4.04
R	0.063	0.083	1.60	2.11
S	0.220	0.240	5.59	6.10
U	0.910	BSC	23.11 BSC	
٧	0.248	0.278	6.30	7.06
W	0.310	0.330	7.87	8.38

STYLE 1: PIN 1. GROUND 2. + OUTPUT 3. + SUPPLY 4. - OUTPUT

**CASE 344C-01 ISSUE B UNIBODY PACKAGE** 



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TITLE:		DOCUMENT NO	): 98ASA99255D	REV: A
8 LD SNSR, DUAL	PORT	CASE NUMBER	R: 1351–01	27 JUL 2005
3 25 3 (6), 5 3 (2)		STANDARD: NO	N-JEDEC	

PAGE 1 OF 2

#### CASE 1351-01 ISSUE A SMALL OUTLINE PACKAGE

#### NOTES:

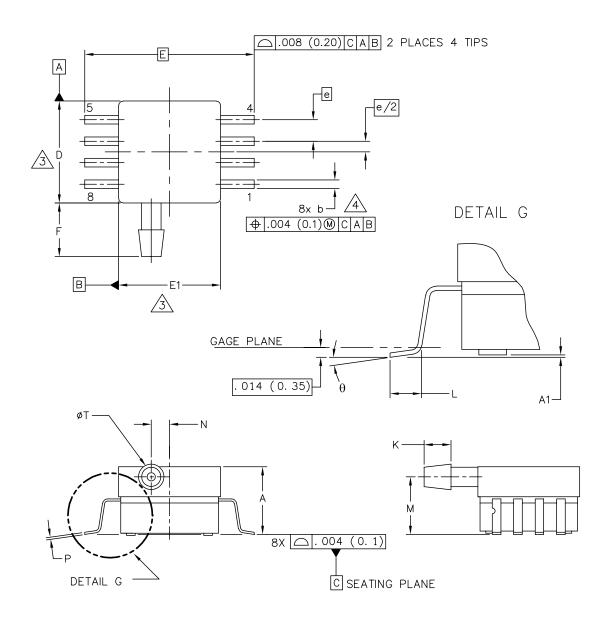
- 1. CONTROLLING DIMENSION: INCH
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.
- DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 MAXIMUM.

STYLE 1:		STYLE 2:	
PIN 1:	GND	PIN 1:	N/C
PIN 2:	+Vou t	PIN 2:	٧s
PIN 3:	٧s	PIN 3:	GND
PIN 4:	−Vout	PIN 4:	Vout
PIN 5:	N/C	PIN 5:	N/C
PIN 6:	N/C	PIN 6:	N/C
PIN 7:	N/C	PIN 7:	N/C
PIN 8:	N/C	PIN 8:	N/C

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8 LD SNSR, DUAL	PORT	CASE NUMBER	R: 1351–01	27 JUL 2005
		STANDARD: NO	N-JEDEC	

PAGE 2 OF 2

CASE 1351-01 ISSUE A SMALL OUTLINE PACKAGE



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8 LD SOP, SIDE PO	ORT CASE NUMBER	R: 1369–01	24 MAY 2005
·	STANDARD: NO	N-JEDEC	

#### CASE 1369-01 ISSUE B SMALL OUTLINE PACKAGE

#### NOTES:

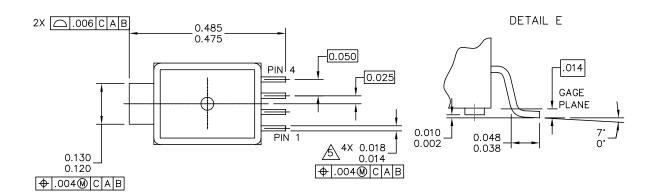
- 1. CONTROLLING DIMENSION: INCH
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- △ DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS.

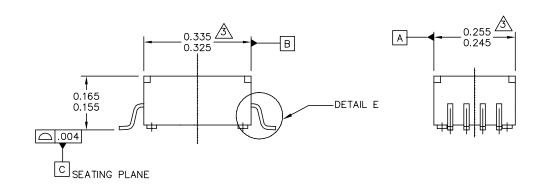
  MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 (0.152) PER SIDE.
- A DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 (0.203) MAXIMUM.

	INC	CHES	MIL	LIMETERS		I	NCHES	MI	LLIMETERS
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
Α	. 300	. 330	7. 11	7. 62	θ	0°	7 <b>°</b>	0°	7°
A 1	. 002	. 010	0. 05	0. 25	_				
b	. 038	. 042	0. 96	1. 07	-				
D	. 465	. 485	11. 81	12. 32	-				
E	. 717	7 BSC	18	.21 BSC	_				
E1	. 465	. 485	11. 81	12. 32	-				
e	. 100	) BSC	2.	54 BSC	_				
F	. 245	. 255	6. 22	6. 47	-				
K	. 120	. 130	3. 05	3. 30	-				
L	. 061	. 071	1. 55	1. 80	_				
М	. 270	. 290	6. 86	7. 36	_				
N	. 080	. 090	2. 03	2. 28	-				
P	. 009	. 011	0. 23	0. 28	-				
Т	. 115	. 125	2. 92	3. 17	-				
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TITLE:					DOC	JMENT NO	): 98ASA99303	3D	REV: B
8 LD SOP, SIDE PORT					CASE NUMBER: 1369-01 24 MAY 2005				
	,					NDARD: NO	N-JEDEC		

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#### CASE 1369-01 ISSUE B SMALL OUTLINE PACKAGE





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5 LD M-PAC	CASE NUMBER	2: 1320-02	22 JUL 2005	
		STANDARD: NO	N-JEDEC	

PAGE 1 OF 2

CASE 1320-02 ISSUE B

#### NOTES:

- 1. DIMENSIONS ARE IN INCHES.
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

 $\sqrt{3}$  DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSION. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .006" PER SIDE.

4. ALL VERTICAL SURFACES TO BE 5' MAXIMUM.

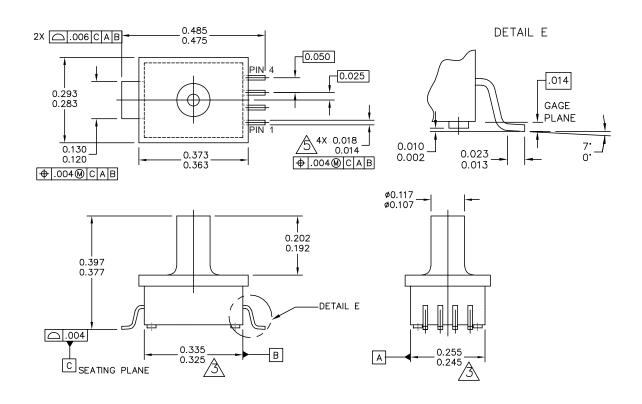
DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 MAXIMUM.

PIN 1: GND +Vout PIN 2: PIN 3: Vs PIN 4: -Vout

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**CASE 1320-02 ISSUE B** 



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5 LD M-PAC, POR	CASE NUMBER	R: 1320A-02	22 JUL 2005	
	STANDARD: NO	N-JEDEC		

PAGE 1 OF 2

CASE 1320A-02 ISSUE A

#### NOTES:

- 1. DIMENSIONS ARE IN INCHES.
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSION. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .006" PER SIDE.

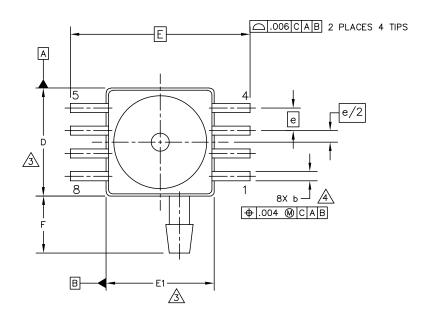
4. ALL VERTICAL SURFACES TO BE 5" MAXIMUM.

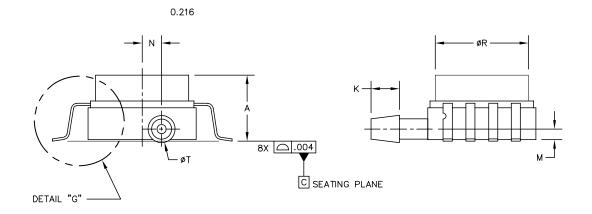
DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 MAXIMUM.

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5 LD M-PAC, PORTE	D CASE NUMBER	CASE NUMBER: 1320A-02 22 JUL 2005		
	STANDARD: NO	N-JEDEC		

PAGE 2 OF 2

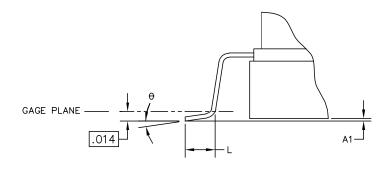
CASE 1320A-02 ISSUE A





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TITLE:		DOCUMENT NO	): 98ASA99302D	REV: B
8 LD SOP, GVP		CASE NUMBER	2: 1368–01	23 MAY 2005
		STANDARD: NO	N-JEDEC	

CASE 1368-01
ISSUE B
SMALL OUTLINE PACKAGE
SURFACE MOUNT



DETAIL	"G"
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TITLE:		DOCUMENT NO	D: 98ASA99302D	REV: B
8 LD SOP, GVP	8 LD SOP, GVP		CASE NUMBER: 1368-01 23 MAY 20	
		STANDARD: NO	DN-JEDEC	

CASE 1368-01 ISSUE B SMALL OUTLINE PACKAGE SURFACE MOUNT

#### NOTES:

- 1. CONTROLLING DIMENSION: INCH
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

 $\stackrel{\triangle}{\bigtriangleup}$  This dimensions does not include mold flash or pprotrusions. Mold flash and protrusions shall not exceed .006 per side.

 $\stackrel{\triangle}{\triangle}$  This dimension does not include dambar protrusion. Allowable dambar protrusion shall be .008 maximum.

STYLE 1: STYLE 2:

PIN 1: GND PIN 2: Vs
PIN 3: Vs PIN 3: GND
PIN 4: -Vout PIN 4: Vout
PIN 5: N/C PIN 5: N/C
PIN 6: N/C PIN 6: N/C
PIN 7: N/C PIN 6: N/C
PIN 8: N/C PIN 8: N/C

	INC	HES	MILLIM	METERS		INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
Α	.280	.300	7.11	7.62	R	.405	.415	10.28	10.54
A1	.002	.010	0.05	0.25	θ	0.	7*	0.	7*
ь	.038	.042	0.96	1.07	-				
D	.465	.485	11.81	12.32	-				
Ε	.690	BSC	17.52	2 BSC	-				
E1	.465	.485	11.85	12.32	-				
е	.100	BSC	2.54 BSC		-				
F	.240	.260	6.10	6.60	-				
κ	.115	.135	2.92	3.43	-				
L	.040	.060	1.02	1.52	-				
М	.035	.055	1.90	2.41	-				
N	.075	.095	0.89	1.39	-				
Р	.009	.011	0.23	0.28	-				
Т	.110	.130	2.79	3.30	-				

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TITLE:	DOCUMENT NO	): 98ASA99302D	REV: B
8 LD SOP, GVP	CASE NUMBER	CASE NUMBER: 1368-01 23 MAY 20	
	STANDARD: NO	N-JEDEC	

CASE 1368-01
ISSUE B
SMALL OUTLINE PACKAGE
SURFACE MOUNT

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